IN THE CLAIMS

1-82 (Canceled).

83. (New) A memory cell, comprising:

a source region in a horizontal substrate;

a drain region in the horizontal substrate;

a channel region separating the source and the drain regions;

an edged defined control gate vertically situated above the channel region and separated from the channel region by a first thickness insulator material;

a first edged defined floating gate horizontally situated above the control gate and separated from the control gate by an intergate dielectric; and

a second edged defined floating gate vertically situated and parallel to one side of the control gate, wherein the second edge defined floating gate is attached to a first end of the first edged defined floating gate and wherein the second edged defined floating gate is separated from the channel region by a second thickness insulator material, the second edged defined floating gate separated from the edged defined control gate by the intergate dielectric.

84. (New) The memory cell of claim 83 further comprising, a third edged defined floating gate vertically situated and parallel to a second side of the control gate, wherein the third edged defined floating gate is attached to a second end of the first edged defined floating gate and wherein the third edged defined floating gate is separated from the channel region by the second thickness insulator material, the third edged defined floating gate is separated from the edged defined control gate by the intergate dielectric.

85. (New) The memory cell of claim 84 wherein a lower end of the edged defined control gate extends below a lower end of the second edged defined floating gate.

86. (New) The memory cell of claim 83 wherein the edged defined control gate has a horizontal width of approximately 100 nanometers (nm).

87. (New) The memory cell of claim 83, wherein the first thickness insulator material is approximately 60 Angstroms (Å), and wherein the second thickness insulator material is approximately 100 Angstroms (Å).

88. (New) The memory cell of claim 83, wherein the first thickness insulator material, the second thickness insulator material, and the intergate dielectric include silicon dioxide (SiO2).

89. (New) The memory cell of claim 83, wherein the edged defined vertical control gate has a vertical height of approximately 500 nanometers (nm) and a horizontal width of approximately 100 Angstroms (Å).

90. (New) The memory cell of claim 83, wherein the intergate dielectric has a thickness approximately equal to the first thickness insulator material.

91. (New) A transistor, comprising:

a horizontal substrate, wherein the substrate includes a source region, a drain region, and a channel region separating the source and the drain region;

an edge-defined vertical control gate separated from a first portion of the channel region by a first oxide thickness;

a first edge-defined vertical floating gate separated from a second portion of the channel region by a second oxide thickness, wherein the first vertical floating gate is parallel to and opposing a first side of the vertical control gate;

a second edge-defined vertical floating gate separated from the second portion of the channel region by the second oxide thickness, wherein the second vertical floating gate is parallel to and opposing a second side of the vertical control gate; and

a horizontal edge-defined floating gate coupled to top portions of the first and second vertical floating gates.

92. (New) The transistor of claim 91, wherein the vertical control gate has a vertical height of approximately 500 nanometers (nm) and a horizontal width of approximately 100 nanometers (nm).

93. (New) The transistor of claim 91, wherein the first oxide thickness is approximately 60 Angstroms (Å), and wherein the second oxide thickness is approximately 100 Angstroms (Å).

94. (New) The transistor of claim 91, wherein the vertical floating gates have horizontal widths of approximately 100 Angstroms (Å).

95. (New) The transistor of claim 91, wherein the horizontal floating gate and the vertical floating gates are separated from the vertical control gate by an intergate dielectric.

96. (New) The transistor of claim 91, wherein a capacitance between the control gate and the floating gates is greater than a capacitance between the floating gates and the channel.

97. (New) A floating gate transistor, comprising:

a horizontal substrate, wherein the substrate includes a source region, a drain region, and a channel region separating the source and the drain region;

two edged defined floating gates connected at their ends and forming a right angle at their connected ends, with one of the floating gates being situated horizontally and another of the floating gates being situated vertically, the vertically situated floating gate separated from the channel region by a first oxide thickness; and

a edged defined control gate vertically situated separated from the two edged defined floating gates by an intergate dielectric, wherein the edged defined control gate is parallel on one side to the vertical situated floating gate, and wherein the edged defined control gate is separated from the channel region by a second oxide thickness.

98. (New) The floating gate transistor of claim 97 further comprising a third edged defined floating gate vertically situated and attached to a different and opposing end of the horizontally situated floating gate, wherein the third edged defined floating gate is separated from the edged defined control gate by the intergate dielectric and separated from the channel region by the first oxide thickness.

99. (Presently Presented) The floating gate transistor of claim 98, wherein the two vertically situated edged defined floating gates and the edged defined control gate vertical gate include polysilicon gates which are separated from one another by silicon dioxide (SiO2).

100. (New) The floating gate transistor of claim 98, wherein the two vertically situated edged defined floating gates and the edged defined control gate vertical gate each have a horizontal width of approximately 100 nanometers (nm).

101. (New) The floating gate transistor of claim 97, wherein the first oxide thickness is approximately 60 Angstroms (Å), and wherein the second oxide thickness is approximately 100 Angstroms (Å).

102. (New) The floating gate transistor of claim 97, wherein the first oxide thickness is approximately equal in thickness to the second oxide thickness.

103. (New) A memory cell, comprising:

a horizontal floating gate coupled to top portions of two opposing vertical floating gates, and wherein the vertical floating gates are parallel with one another; and

a non-coupled vertical control gate separated from the two vertical floating gates and the horizontal floating gate by a intergate dielectric, wherein the non-coupled vertical control gate is interposed between the two vertical floating gates.

104. (Presently Presented) The memory cell of claim 103 wherein the two vertical floating gates are separated from a channel region by a first oxide thickness.

105. (New) The memory cell of claim 104 wherein the control gate is separated from the channel region by a second oxide thickness.

106. (New) A memory cell comprising:

a horizontal floating gate coupled to the ends of two opposing and parallel vertical floating gates; and

a vertical control gate that is separated from the floating gates by an intergate dielectric, and wherein the vertical gate is also parallel to and is interposed between the two parallel vertical floating gates.

107. (New) The memory cell of claim 106 wherein the gates are located above a channel region for the memory cell.

108. (New) The memory cell of claim 106 wherein the channel region separates source and drain regions of a horizontal substrate for the memory cell.

109. (New) A transistor comprising:

a first floating gate horizontally situated;

a second floating gate vertically situated;

a third floating gate vertically situated; and

a control gate vertically situated;

wherein the floating gates surround the control gate on three sides of the control gate and are separated from the control gate by an intergate dielectric, and wherein at least two of the floating gates are separated by and parallel to the control gate.

110. (New) The transistor of claim 109 wherein the second and third floating gates and the control gate are separated from a channel region by a same oxide thickness.

111. (New) The transistor of claim 109 wherein the second and third floating gates are separated from a channel region by a different oxide thickness than the control gate.

112. (New) A transistor comprising:

three coupled floating gates coupled on their ends with one another, where two of the coupled floating gates are parallel with one another; and

a non-coupled control gate surrounded on three sides by the three coupled floating gates and interposed between the two parallel floating gates, and further separated by an intergate dielectric from the three coupled floating gates.

113. (New) The transistor of claim 112 wherein the two parallel floating gates are coupled indirectly with one another through the remaining coupled floating gate.

114. (New) The transistor of claim 112 wherein the two parallel floating gates are separated from a channel region by a first oxide thickness and the control gate is separated from the channel region by a second oxide thickness.